

U.S.S.N. 10/729,034

Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to overcome Examiners objections.

The claims have been amended and new claims added to more clearly claim Applicants invention.

Support for the amended claims is found in the original claims and/or the Specification. No new matter has been added.

For example support for new claims 22-25 are found in the Specification particularly with respect to Figure 1E.

Claim Rejections under 35 USC 102

1. Claims 1, 3, 5-8, and 11 stand rejected under 35 USC 102(e)

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as being anticipated by Kiyotoshi (US Pub 2004/0152258).

Kiyotoshi discloses a stacked capacitor structure e.g., Figures 9 and Figure 18 having a series of stacked layers in the form of electrodes/capacitor dielectric/electrode where the stacked layers are covered by a single insulating layer (128) (e.g., disposed in a single IMD layer). As shown in figure 9, two capacitors are formed by common electrical connection of a lower electrode 121a and an upper electrode 125c where a middle electrode 123a acts as both an upper electrode for the lower first capacitor structure and a lower electrode for the upper capacitor structure.

Thus, the two capacitor structure of Kiyotoshi differs from Applicants disclosed and claimed invention in several ways.

Kiyotoshi does not disclose:

"a first MJM capacitor structure disposed in a first IMD layer comprising a first upper electrode and a first lower electrode; and,

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at least a second MIM capacitor structure arranged in stacked relationship in an overlying IMD layer comprising a second upper electrode and second lower electrode separate from said first upper and first lower electrode to form an MIM capacitor stack;

wherein, the first lower electrode is arranged in common electrical signal communication comprising electrically communicating vias with the second upper electrode and the first upper electrode is arranged in common electrical signal communication with the second lower electrode to form said MIM capacitor stack in parallel electrical relationship."

For example, Kiyotoshi does not disclose a first and second IMD layers as Applicants have disclosed and claimed and does not disclose first lower and upper electrodes in the first IMD layer and second lower and upper electrodes **separate from the first lower and upper electrodes** in the overlying IMD layer as Applicants have disclosed and claimed.

In Figure 18, Kiyotoshi discloses a similar structure but having 5 stacked electrode layers separated by four capacitor

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dielectric layers to form four capacitor structures. In this embodiment the electrode layers (202a, 204a, 206a, 208a, and 210a) are separated by capacitor dielectric layers (203, 205, 207, and 209) where the stacked layers are covered by a single IMD (insulating) layer (214) (e.g., disposed in a single IMD layer). Electrical contacts (vias) are provided extending through the **single insulating layer** to provide common electrical connection to alternating electrode layers. Electrodes 204a, 206a, and 208a act **as both upper and lower electrodes** in the stacked capacitor structure.

Thus, Kiyotoshi is clearly insufficient to anticipate Applicants disclosed and claimed invention.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"The identical invention must be shown in as complete

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detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants note and appreciate Examiners indication of allowable subject matter in claims 2, 4, 9, and 10, and have incorporated allowable subject matter in new claims 26 through 31.


Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

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Respectfully submitted,

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